

CI13241 Datasheet

High performance neural network intelligent voice chip



- **Neural Network Processor (BNPU)**

-BNPU V3.5 supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, this processor can realize high-performance speech recognition and speech noise reduction functions

- **CPU and memory**

-CPU frequency up to 210 MHz
-Built-in 1MBytes Flash memory
-Built-in 288KBytes SRAM
-Built-in 256bit eFuse for application encryption

- **Audio Codec**

-High performance and low power consumption audio ADC, $\text{SNR} \geq 95\text{dB}$
-Low power consumption audio DAC, $\text{SNR} \geq 95\text{dB}$

- **PWM**

-Supports 4 PWM interfaces

- **GPIO**

-13 high-speed GPIO with a switching frequency of up to 20MHz
-7 GPIO supports 5V input

- **Reset and power management**

-Power supply voltage range 3.6V~5.5V
-Built-in PMU power management unit
-Built-in power-on reset (POR)
-Built-in voltage detection (PVD)

- **clock**

-Built-in RC oscillator
-Support for external crystal oscillator input

- **communication interface**

-1 IIC interface
-3 UART interfaces, support 5V communication, support up to 3Mbps rate

- **Timer and watchdog**

-Built-in 2 sets of 32-bit timers and 1 watchdog

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1 summary

1.1 Functional description

CI13241 is a next-generation high-performance neural network intelligent voice chip developed by Chipintelli. It integrates the company's proprietary Brain Neural Network Processor (BNPU) V3.5 and CPU core, delivering a system clock rate of up to 210MHz. Featuring 288KB of built-in SRAM, it incorporates a PMU power management unit and RC oscillator, along with a single-channel high-performance low-power Audio Codec and multiple peripheral control interfaces including UART, I2C, PWM, and GPIO. The chip requires minimal external components like resistors and capacitors to develop various smart voice product hardware solutions, offering exceptional cost-effectiveness.

CI13241 adopts industrial-grade design standards, has high environmental reliability, its working environment temperature range is $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$, in line with MSL3 level of humidity sensitivity, in line with IEC 61000-4-2 of 4KV contact discharge test standard, in line with FCC electromagnetic compatibility standard, in line with ROHS and REACH environmental protection standards.

The CI13241 utilizes Chipintelli's 3.5th-generation BNPU technology, which supports neural networks including DNN, TDNN, RNN, and CNN, along with parallel vector operations. This enables high-performance speech recognition, noise reduction, and exceptional environmental noise suppression capabilities. The CI13241 solution also supports multiple global languages such as Chinese, English, and Japanese, making it widely applicable in home appliances, lighting, toys, wearables, industrial equipment, automotive products, and other fields. It facilitates voice interaction control and supports various intelligent voice application scenarios.

1.2 Chip specifications

The function block diagram of CI13241 chip is shown in the figure below:

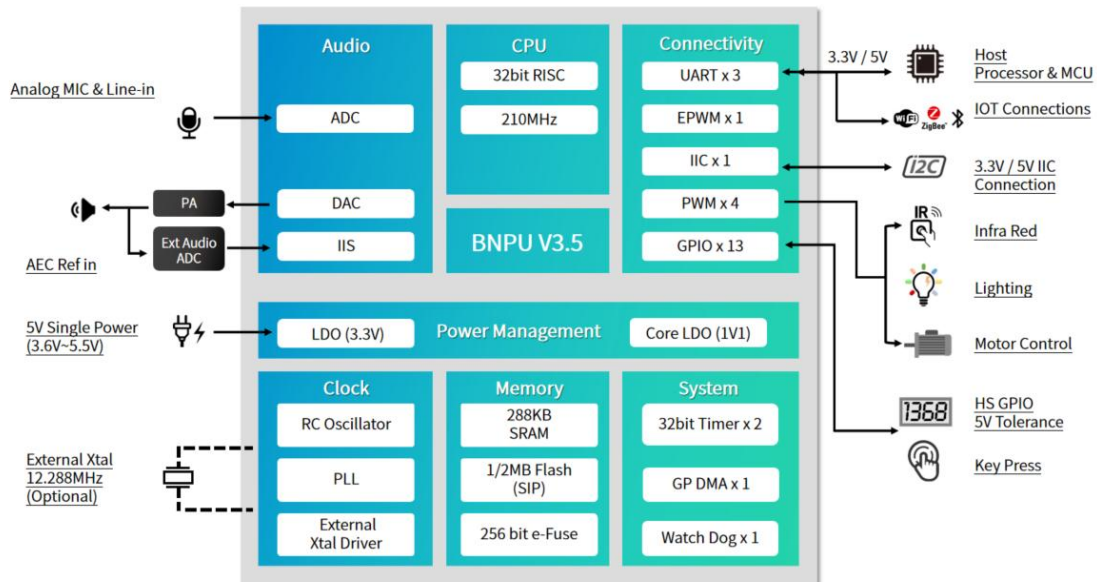


Figure 1: CI13241 function block diagram

■ Brain neural network processor BNPU V3.5

-BNPU V3.5 supports DNN\TDNN\RNN\CNN and other neural network, parallel vector operations, which can realize high-performance speech recognition, speech noise reduction and other functions

■ CPU

- 32-bit high-performance CPU, running at up to 210MHz
- 32-bit single-cycle multiplier, supporting DSP expansion acceleration

■ Memory

- Built-in 288KB SRAM
- Built-in 256bit eFuse
- Built-in 1MB Flash

■ Audio interface

- Built-in high performance low power Audio Codec module, supporting single channel ADC sampling and single channel DAC playback
- Support for Automatic Level Control (ALC) function
- Support for 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rate

■ PMU power management unit

-Built-in 2 high-performance LDO, no need to configure external power chip, only a small number of peripheral components are required

-Support wide power supply voltage, power supply range 3.6V~5.5V

■ Clock

-Built-in RC oscillator

■ Peripheral and timer

-3 UART ports, up to 3M baud rate

-1 IIC interface, which can be expanded by external IIC devices

-4 PWM interfaces, which can be directly driven for lamp control and motor applications

-2 built-in 32-bit timers

-Built-in 1 independent watchdog (IWDG)

■ GPIO

-Supports 13 GPIO ports and can be used as a master control IC

-Each GPIO port can be configured to interrupt, and pull up and pull down can be configured

-7 GPIO channels support wide voltage 5V level signal communication directly, without external level conversion, only need to be connected to a pull-up resistor to 5V

■ Software development support

-Provides complete software development kit, application solution examples and voice development platform online firmware production functions, details please visit:

<https://aiplatform.chipintelli.com>

■ Firmware burning and protection

-Support UART upgrade and firmware protection

■ EMC and ESD

-Internal ESD enhanced design, can pass 4KV contact discharge test

■ ROHS and REACH

-Use of environmentally friendly materials, support through ROHS and REACH tests

■ Packaging and operating temperature range

-Packaging form: SSOP24, size 8.6mm long, 6mm wide and 1.64mm high

-Working environment temperature: -40°C~ + 85°C

2 Pin diagram and function description

2.1 Pin diagram

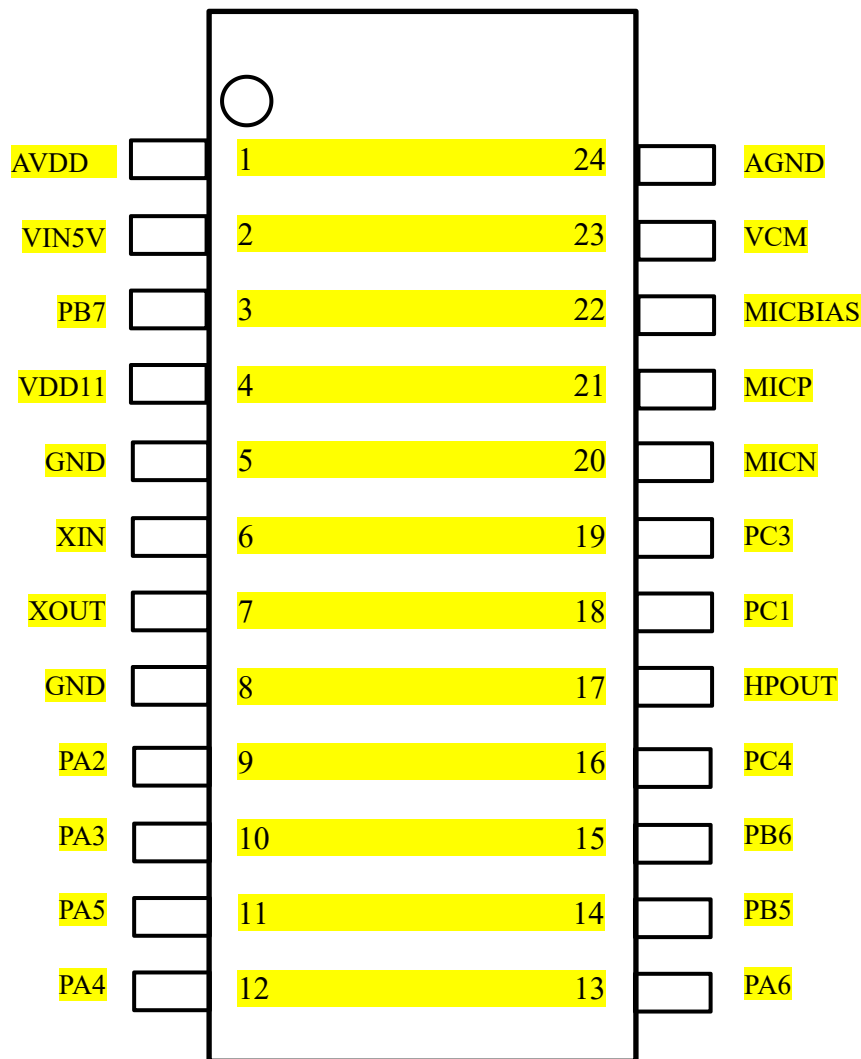


Figure 2: SSOP24 pin diagram

2.2 Pin description

Table 1: Pin description

Pin number	Pin Name	Type	5V-- Tolerant	Power on default state	Description Alternate functions
1	AVDD	P	-	-	<ul style="list-style-type: none"> ● Internal LDO-3.3V Output ● Internal analog circuitry is powered by 3.3V input ● * Note1*
2	VIN5V	P	-	-	<ul style="list-style-type: none"> ● Power supply voltage input, power supply voltage range 3.6V~5.5V ● * Note1*
3	PB7	IO	-	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB7
4	VDD11	P	-	-	<ul style="list-style-type: none"> ● LDO-1.1V output ● The kernel is powered by 1.1V input ● * Note1*
5	GND	P	-	-	Ground
6	XIN	I	-	-	<ul style="list-style-type: none"> ● XIN (default state of power-on) ● GPIO PA0 ● PWM2
7	XOUT	O	-	-	<ul style="list-style-type: none"> ● XOUT (default on power-on state) ● GPIO PA1
8	GND	P	-	-	Ground
9	PA2	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA2 (default state on power-on) ● IIS_SDI ● IIC_SDA ● UART1_TX ● PWM0 ● PWMP
10	PA3	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA3 (default on power-on state) ● IIS_LRCLK ● IIC_SCL ● UART1_RX1 ● PWM1 ● PWMN
11	PA5	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA5 (default on power-on state) ● IIS_SCLK ● - ● UART2_TX ● PWM3 ● PWMN
12	PA4	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PA4 (default on power-on state)/PG_EN (programming function is activated when high voltage is applied during power-on) ● * Note2* ● IIS_SDO ● - ● - ● PWM2 ● PWMP

13	PA6	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA6 (default state on power-on) ● IIS_MCLK ● - ● UART2_RX ● PWM0
14	PB5	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB5 (default state on power-on) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
15	PB6	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB6 (default state on power-on) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
16	PC4	IO	-	IN, T+U	<ul style="list-style-type: none"> ● Retained (default state on power-on) ● GPIO PC4 ● SCL ● PWM0
17	HPOUT	O	-	-	DAC output
18	PC1	IO	-	IN, T+D	<ul style="list-style-type: none"> ● Retained (default state on power-on) ● GPIO PC1 ● 3.TX2 ● PWM3
19	PC3	IO	-	IN, T+D	<ul style="list-style-type: none"> ● Retained (default state on power-on) ● GPIO PC3 ● SDA ● PWM1
20	MICN	I	-	-	Microphone N input
21	MICP	I	-	-	Microphone P input
22	MICBIAS	O	-	-	Microphone bias output
23	VCM	O	-	-	VCM Output
24	AGND	P	-	-	Analog ground

Note1 The pin needs to be connected to an external 4.7uF capacitor

Note2 When power on, this pin is high level, and the system will enter programming mode

Symbol definition

I input

O output

IO bidirectional

P power or ground

T+D Tri-state pull-down

T+U Tri-state pull-up

OUT power-on defaults to output mode

IN power-on defaults to input mode

All IOs can be configured with drive capability and pull-up/down status.

2.3 Function multiplexing

Table 2: IO multiplexing function

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
XIN	PA0	PWM2					XIN
XOUT	PA1						XOUT
PA2	PA2	SDI	IIC_SDA	UART1_TX	PWM0	PWMP	
PA3	PA3	LRCK	IIC_SCL	UART1_RX	PWM1	PWMN	
PA4	PA4	SDO	-	-	PWM2	PWMP	PG_EN Note1
PA5	PA5	SCLK		TX2	PWM3	PWMN	
PA6	PA6	MCLK		RX2	PWM0		
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP		
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN		
PC4	-	PC4	SCL	PWM0			
PC1	-	PC1	TX2	PWM3			
PC3	-	PC3	SDA	PWM1			

Note 1: The PA4 (PG_EN) pin on the chip is internally pulled up by default. When the system detects a high level at this pin during power-on and receives upgrade signal information from the UART0 interface, it automatically enters upgrade mode. In this state, the accompanying upgrade tool can be used to program the chip's internal Nor Flash. If no upgrade signal is detected from the UART0 interface, the system will enter normal startup mode.

3 Chip interface description

3.1 General Input Output (GPIO)

3.1.1 Brief introduction

GPIO (General IO Interface) is a general-purpose input/output port that allows devices to interact with peripheral hardware at level signals. It can be used as an input to receive external signals or as an output to control peripheral hardware.

3.1.2 Characteristic

The CI13242 chip supports multiple programmable I/O pins (configurable

through software individually). Each GPIO port is equipped with corresponding control and configuration registers, enabling precise control and status monitoring of peripheral hardware by independently activating or deactivating individual pins. The chip features three GPIO groups (GPIO0, GPIO1, and GPIO2), where GPIO0 corresponds to the PA port, GPIO1 to the PB port, and GPIO2 to the PC port. For detailed pin assignments for each group, please refer to Section 2.2's Pin Description section.

CI13242 provides a series of interfaces including IO input/output status query, interrupt shielding, interrupt shielding status check, interrupt clearing, interrupt status inquiry, and interrupt trigger mode configuration (supporting low-level, high-level, rising-edge, falling-edge, or both-edge triggering) to meet diverse application scenarios and requirements.

3.2 Universal Asynchronous Receiver Transmitter (UART)

3.2.1 Brief introduction

UART is a universal asynchronous serial communication data interface that enables data reception and transmission between two devices, supporting full-duplex communication. There is no shared clock signal between the receiving and sending devices. To ensure communication reliability, both devices need to set the same baud rate and data frame format.

CI13242 supports 3 UART controllers: UART0, UART1 and UART2.

3.2.2 Characteristic

- Supports the standard UART protocol. The data frame format consists of four parts: start bit, data bit (length can be configured), parity bit (optional) and stop bit (width can be configured). The baud rate can be configured.
- When the bus is idle, the signal line is high.
- Start: used to identify the start of a data frame. Each data frame starts with an output of a bit width low level from the sender, notifying the receiver that the data transmission has started;
- Data bit: The length of the transmitted data can be configured by UART_LCR register to 5~8 bits, usually 8 bits. The bit transmission order is low priority,

sending the lowest bit LSB first and the highest bit MSB last;

- Parity check: The parity check function can be enabled or disabled through the UART_LCR register. When the parity check function is enabled, the parity check can detect whether there is an error in data transmission after the completion of data bit transmission;
- Stop bit: used to identify the end of the transmitted data frame. Each data frame ends with a high level, and the length can be configured as 1, 1.5, or 2 bits through UART_LCR register;

3.2.3 Sequence chart

The timing diagram of UART data transmission of one data frame (8-bit data bit, parity bit, 1bit stop bit) is as follows:

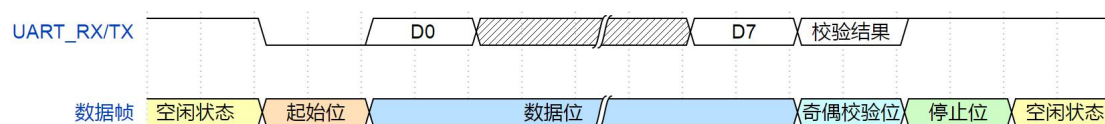


Figure 3: Data frame timing diagram 1

The timing diagram of UART data transmission of one data frame (start bit, 7-bit data bit, parity bit, 1.5bit stop bit) is as follows:

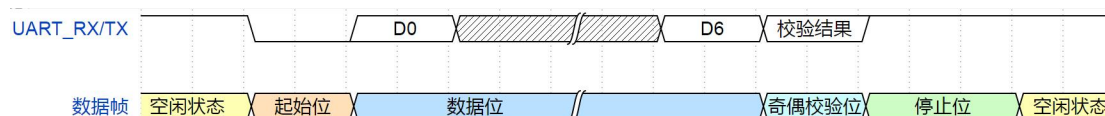


Figure 4: Data frame timing diagram 2

The timing diagram of UART data transmission of one data frame (start bit, 8-bit data bit, no parity bit, 2-bit stop bit) is as follows:

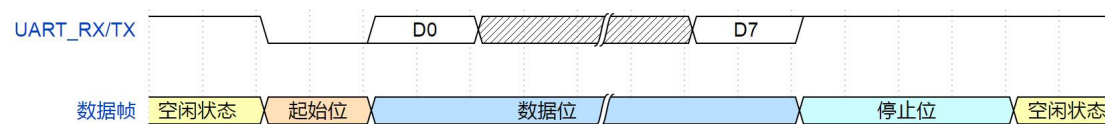


Figure 5: Data frame timing diagram 3

The higher the UART baud rate is set, the faster the data transmission speed will be, but it will also increase the interference and bit error rate. When setting the baud rate, we need to consider whether the serial port hardware of both sides of communication supports this baud rate. If the baud rate is set too high, the data transmission may be unstable.

Supports a maximum baud rate of 3Mbps, which can be configured through UART_I_BRD and UART_F_BRD registers.

3.3 Pulse width modulation output (PWM)

3.3.1 Brief introduction

PWM (Pulse Width Modulation) is a technology that simulates the level of analog signal by adjusting the duty ratio (the proportion of high level time in the whole cycle) of digital pulses. It is widely used in motor control, power supply management, LED dimming and other fields.

CI13242 has 4 dedicated PWM. The frequency of each PWM output signal is configured by timer SC register, and the duty cycle of each PWM output signal is configured by timer SPWMC register. 100% duty cycle is not supported (often high). If 100% duty cycle is required, it can be achieved by configuring GPIO.

3.3.2 Characteristic

- Counting clock division, supporting 1, 2, 4 and 16 division, which can be configured through timer CFG register;
- Supports two 32-bit decrement counters;
- Variable duty cycle PWM pulse width waveform output;
- The output level polarity after support stop is configured through timer restart MD register;

3.4 General Timer (TIMER)

3.4.1 Brief introduction

The Timer (GENERAL Timer) is a 32-bit decrementing counter featuring configurable frequency divider and multiple counting modes. It triggers a timing event when the count reaches zero, commonly used to repeatedly trigger timer events within specified time intervals. This component can serve as both a periodic interrupt generator and event counter. The CI13242 contains two identical dedicated timers (TIMER0~TIMER1) that support cascaded operation.

3.4.2 Characteristic

- Supports three counting modes, which can be configured through the timer_CFG register: single-cycle counting mode, automatic reload counting mode and free running counting mode;
 - Single-cycle counting mode: The timer counts only one counting cycle;
 - Automatic reload count mode: The counter is reinitiated at the end of each count;
 - Free running count mode: The count value cycles from 0xFFFFFFFF to 0x00000000 at the end of each count;
- Counting clock division, supporting 1, 2, 4 and 16 division, which can be configured through timer CFG register;
- 32-bit decrementing counter, which can read the real-time value of the counter and read it through the timer CC register;
- Supports cascaded mode configuration, which is configured through timer cfg0 register;
- Support interrupt when counting is completed and reported;

3.5 Audio Digital Transmission Bus (IIS)

3.5.1 Brief introduction

IIS is a communication interface used to transmit audio data between digital audio devices, and realizes the signal transmission function of external 16/20/24/32bit stereo digital audio signal codec circuit.

The CI13242 features three IIS channels: IIS0 through IIS2. Specifically, IIS0 serves as a general-purpose IIS with both TX (transmission) and RX (reception) capabilities, enabling communication with other chips via PAD. IIS1 functions as an internal dedicated IIS within the chip, containing separate TX and RX units. The TX unit specifically supports the internal CODEC DAC of the CI13242, while the RX unit serves the CODEC ADC. IIS2 is a specialized IIS channel exclusively designed for RX functionality.

CI13242 supports dedicated IISDMA for data transfer between memory and IIS. All IIS share a single IISDMA0, and each IIS uses a different channel of IISDMA0.

3.5.2 Characteristic

- The IIS interface is composed of MCLK, SCK, LRCLK, SDI and SDO signal lines;
- MCLK: The main clock, which is usually 128/192/256/384 times of the audio sampling rate (the frequency of LRCLK);
- SCK: serial bit clock, 1bit data is transmitted in each SCK cycle;
- LRCLK: Frame clock, used to switch data between left and right channels;
- In IIS format, LRCLK is 0 to indicate that the current data frame is left channel data, and 1 to indicate that the current data frame is right channel data;
- In left/right alignment format, LRCLK is 0 to indicate that the current data frame is right channel data, and 1 to indicate that the current data frame is left channel data;
- SDI/SDO: serial data input/output, used to transmit audio data;
- The ratio of LCLK to SCK can be configured to 1:32 or 1:64 through IISRX0CTRL/IISTX0CTRL registers;
- The data format can be configured as IIS format, left aligned format and right aligned format through IISRX0CTRL/IISTX0CTRL registers;
- The number of bits for sending and receiving data can be configured as 16bit, 20bit, 24bit and 32bit through IISRX0CTRL/IISTX0CTRL registers;
- In single-channel mode, the function of copying channel data is supported. When sending, the single-channel data is sent to both left and right channels at the same time, and when receiving, the left and right channels are merged into a single-channel data;
- When the sampling data bit width is 16bit, the channel data merging function is supported. The specific functional principle is shown in the figure below;

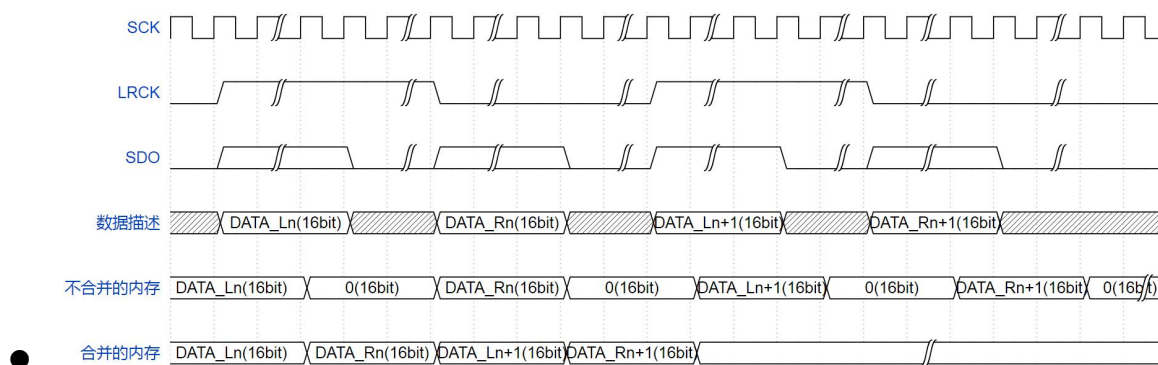


Figure 6: Schematic diagram of channel merging function

- When receiving and sending data, the left and right channel data support switching. The switching of received left and right channel data is configured through IISRX0CTRL register, and the switching of sent left and right channel data is configured through IISTX0CTRL register;
- The data receiving and sending channels are completely independent;
- Supports silent mode, which is configured through IISRX0CTRL register for receiving and IISTX0CTRL register for sending;
- Supports the configuration of single channel and dual channel. During reception, the IISRX0CTRL register is used to configure single channel or dual channel, and during transmission, the IISTX0CTRL register is used to configure single channel or dual channel;

3.6 Integrated Circuit Bus (IIC)

3.6.1 Brief introduction

The I2C interface is a bidirectional dual-wire synchronous serial bus that includes the SDA (Serial Data Line) and SCL (Serial Clock Line), both featuring open-drain outputs. This bus is commonly used for communication between one or more master devices and one or more slave devices. Each device connected to the bus has a unique address, and only one master device can initiate access requests to a slave device at any given time.

CI13242 supports 1 IIC. Its data frame format is usually composed of five parts: start signal, address signal, response signal, data signal and stop signal. It supports two modes: standard transmission rate of 100kbit/s and fast transmission rate of 400kbit/s.

3.6.2 Description of characteristics

- SDA: serial data line, two-way I/O line;
- SCL: serial clock line, provided by master;
- Support master and slave mode register configuration;
- Master: Starts the bus to transmit data and generates a clock when acting as a master device;
- Slave: A slave device that is addressed as a slave device and has a unique address;

- Starting signal: When SCL is high, SDA jumps from high to low, indicating the start of transmission;
- Address signal: supports 7-bit addressing mode, including 7bit address bit and 1bit read/write bit;
- Response signal: ACK for successful reception, NACK for failure or end of transmission;
- Data signal: transmitted by Byte, the MSB is sent first and the LSB is sent last;
- Stop signal: When SCL is high, SDA jumps from low level to high level, indicating the end of transmission;
- The bus transmission rate can be configured as standard-100kbit/s and fast-400kbit/s;

3.6.3 Sequence chart

The master initiates communication by generating the Start condition: When SCL is high, it pulls SDA low and transmits 8 clock pulses through SCL to transfer a Byte containing 7-bit address bits and 1-bit read/write bits. If the slave's address matches the transmitted 7-bit address, a response signal is generated. Both master and slave determine whether to transmit or receive data based on the read/write bits, and conclude transmission by checking the logic level of the response bit. During data transfer, SDA changes only when SCL is low. Upon completing communication, the master sends the Stop condition to terminate transmission: When SCL is high, it pulls SDA high.

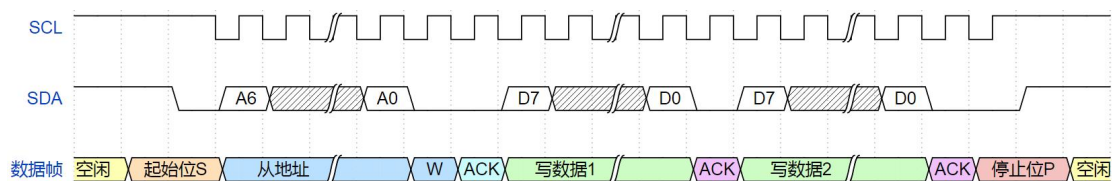


Figure 7: Continuous data write operation timing diagram

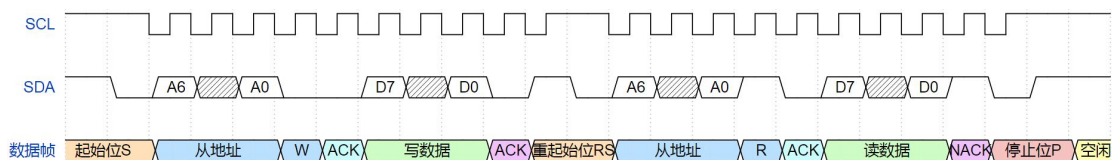


Figure 8: Write before read operation timing diagram

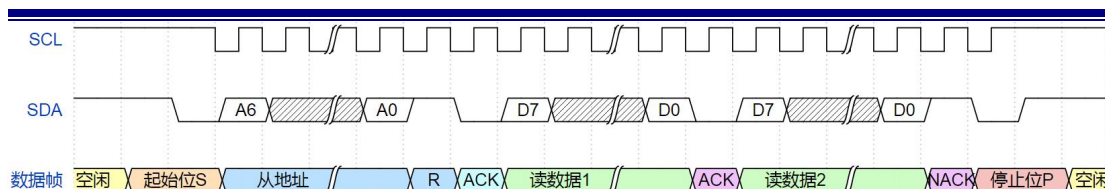


Figure 9: IIC read operation timing diagram

3.7 Independent Watchdog (IWDG)

3.7.1 Brief introduction

IWDG is a hardware timing circuit, which is mainly used to monitor the system faults caused by abnormal operation and recover from the faults.

3.7.2 Characteristic

CI13242 supports 1 IWDG module. IWDG is based on a 32-bit decrementing counter, which starts to decrement from the loaded value. When the count value reaches 0, an timeout interrupt is generated. The counter reloads the loaded value again, and when the count value reaches 0 again, if the timeout interrupt is not cleared, IWDG will generate a reset request.

The range of the reset field can be configured through the SYS_RESET_CFG register.

3.8 Multimedia audio and video codec (CODEC)

3.8.1 Brief introduction

CI13242 has built-in high-performance low-power audio CODEC, which supports one ADC and one DAC. The analog signal input by MIC is amplified by PGA after MIC gain. This PGA can be controlled by ALC of CODEC itself, and digital gain can be amplified after PGA.

3.8.2 Characteristic

- DAC supports up to 24bit, SNR up to 90dB;
- ADC supports up to 24 bits, SNR up to 90dB;

- Support single-ended, differential MIC input and line-in input;
- Support ALC automatic gain control;
- Sampling rate support: 8k/12k/16k/24k/32k/44.1k/48k;

3.9 Enhanced Pulse Width Modulation output (EPWM)

3.9.1 Brief introduction

EPWM (Enhanced Pulse Width Modulation output) is a more sophisticated pulse width modulation technology compared to conventional PWM, offering enhanced functionality and configuration options. It enables specialized functions such as reverse operation, chopping, low-level or high-level phase control, and is widely used in power control devices across industrial and consumer electronics applications, including motor control systems and switching power supplies.

Each EPWM consists of two PWM outputs, PWMN and PWMP, respectively. This pair of PWM outputs can be used as a normal PWM, complementary PWM wave output, or custom PWM output.

3.9.2 Characteristic

- A 16-bit counter with controllable frequency;
- Supports external or software to configure the start or end of a counter through the TBCTL register;
- Support for one to multiple PWM outputs: central symmetric PWM output; edge symmetric PWM output; edge asymmetric PWM output;
- Support initial phase configuration through TBPHS register;
- 16-bit dead time, which supports the delay time of rising edge or falling edge through DBRED or DBFED registers;
- When the external brake command arrives, the PWM output can be configured as high level, low level and high resistance state through TZSEL register;

3.9.3 Description of configuration values

The core configuration parameters of EPWM include TBPRD, ZERO, CMPA

and CMPB. Among them, TBPRD defines the period length of PWM wave, while CMPA and CMPB are used to set the duty ratio. By configuring these parameters, the frequency and duty ratio of PWM wave can be controlled.

- TBPRD: Count cycle value (>0), the maximum configuration width is 16 bits, and the action of pull high, pull low or unchanged is generated when the count is configured to TBPRD value through AQCTLA or AQCTLB register;
- ZERO: Counting cycle value ($=0$), which is configured by AQCTLA or AQCTLB register to generate pull high, pull low or unchanged actions when counting to ZERO value;
- CMPA: Count comparison value A, the maximum configuration width is 16 bits, and when the count is configured to CMPA value through AQCTLA or AQCTLB register, it generates pull high, pull low or unchanged actions;
- CMPB: Count comparison value B, the maximum configuration width is 16 bits. When the count is configured to CMPB value through AQCTLA or AQCTLB register, it generates actions such as pull high, pull low or unchanged;

3.9.4 Counting patterns

EPWM supports three counting modes: increment mode, decrement mode, and add/subtract mode. Different counting modes are suitable for different application scenarios.

- Increasing mode: The counter increases from 0 to TBPRD every cycle. One TBPRD cycle can output one PWM cycle, which can be configured through TBCTR register;
- Decrement mode: The counter decreases from TBPRD to 0 every cycle. One TBPRD cycle can output one PWM cycle, which can be configured through TBCTR register;
- Add/subtract mode: The counter increases from 0 to TBPRD in odd cycles and decreases from TBPRD to 0 in even cycles. Two TBPRD cycles can output one PWM cycle, which can be configured through TBCTR register;

3.9.5 Usage method

EPWM can output various waveforms through configuration, including 50% duty cycle PWM waves and low-level duty cycle PWM waves. To generate the

desired waveform, users must first configure the values of TBPRD, CMPA, and CMPB, specify their counting modes, and define actions triggered when the counter reaches specific thresholds (TBPRD, ZERO, CMPA, CMPB). This configuration process allows three possible scenarios: $CMPA = CMPB$, $CMPA > CMPB$, or $CMPA < CMPB$.

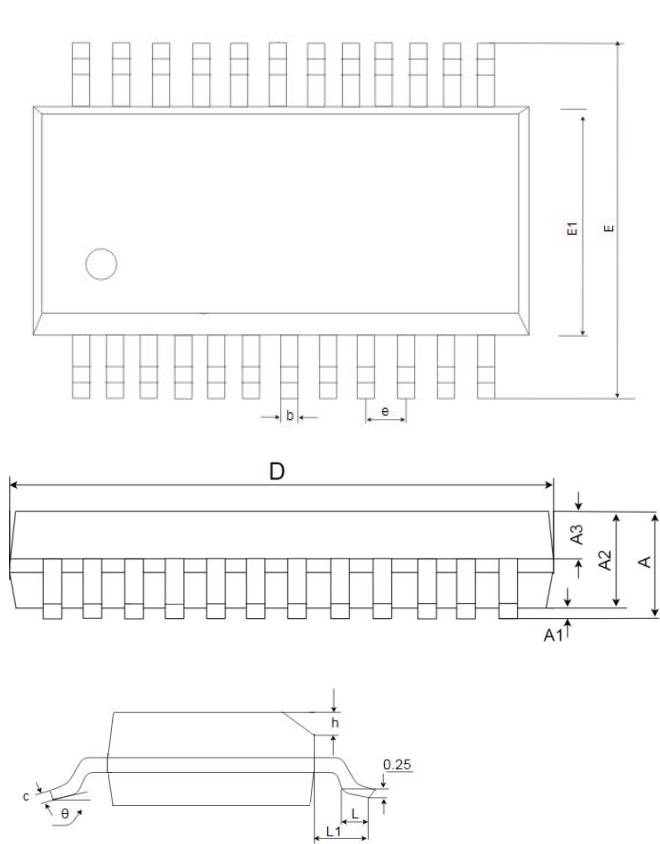
4 electrical character

Table 3: Electrical characteristics table

symbol	description	least value	representative value	crest value	unit
VIN5V	Chip power input *Note1*	3.6	5	5.5	V
AVDD	3.3V power supply	2.97	3.3	3.63	V
VDD11	1.1V power supply	0.99	1.1	1.21	V
V_{IH}	Enter high voltage, $3.0V \leq AVDD \leq 3.6V$	$0.7 \times AVDD$	-	$AVDD + 0.3$	V
V_{IL}	Input low voltage, $3.0V \leq AVDD \leq 3.6V$	-0.3	-	$0.3 \times AVDD$	V
V_{OL}	Output low voltage @IOL = 12mA	-	-	0.4	V
V_{OH}	Output high voltage @IOH = 20mA	2.4	-	-	V
I_{5VIO}	IO (5V withstand voltage) output 3.3V with drive current	20	-	33	mA
I_{33VIO}	IO(3.3V (Voltage withstand) Drive current when output 3.3V	14	-	24	mA
$\Sigma IVDD$	The total current of all IOs in the chip	-	-	260	mA
Pde	Using 5V power supply, the chip 1.1V is powered by an external DC-DC chip. The total power consumption of the 5V input during normal identification (environmental temperature TA = 25 °C)	40	-	90	mW
Pdi	The chip is powered by 5V and uses an internal PMU. The total power consumption of the 5V input is recognized normally	125	-	255	mW

	(environmental temperature $T_A = 25\text{ }^{\circ}\text{C}$)				
RC Precision	$T_A = -40\text{ to }85^{\circ}\text{C}$	-1.5	-	+1.5	%
T_A	The chip uses an internal RC oscillator to adapt to the operating temperature	-40	-	+85	$^{\circ}\text{C}$
T_{ST}	Chip storage temperature	-55	-	+150	$^{\circ}\text{C}$

5 Packaging information



COMMON DIMENSIONS

SYMBOL	UNIT: MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.48	1.50
A3	0.6	0.65	0.70
b	0.23	—	0.31
c	0.20	—	0.24
D	8.55	8.6	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

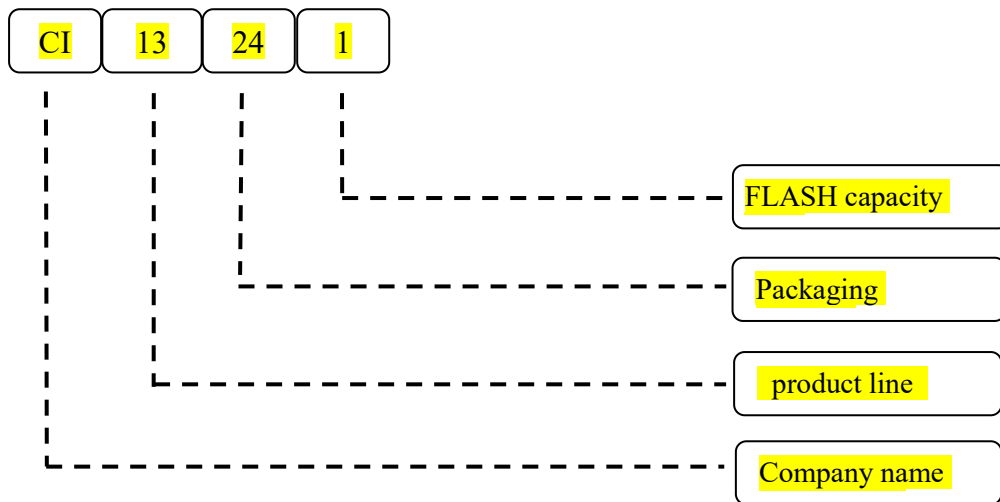
Figure 10: Package size

6 Order information

The screen printing of CI13241 chip is shown in the figure below. The first line is the company LOG, the second line is the chip model, the third line is the production batch number, and the dot in the lower left corner is the identification of pin 1.



The chip model is defined as follows:



Chip model	Package Type	Basic packaging	Package Qty	Ex-factory packaging	Standard Pack Qty
CI13241	SSOP24	Fitting	50pcs	box-packed	10000pcs (200 tubes/box)

Table 4: Order Information Table

7 Application program

7.1 Application reference circuit diagram

The CI13241 chip requires minimal peripheral components to support various voice applications, accommodating both single-microphone differential and single-ended input configurations. Users can select optimal design solutions based on application requirements regarding functionality, power consumption, and cost considerations. Below is a detailed description of its application circuit diagram using a typical implementation example.

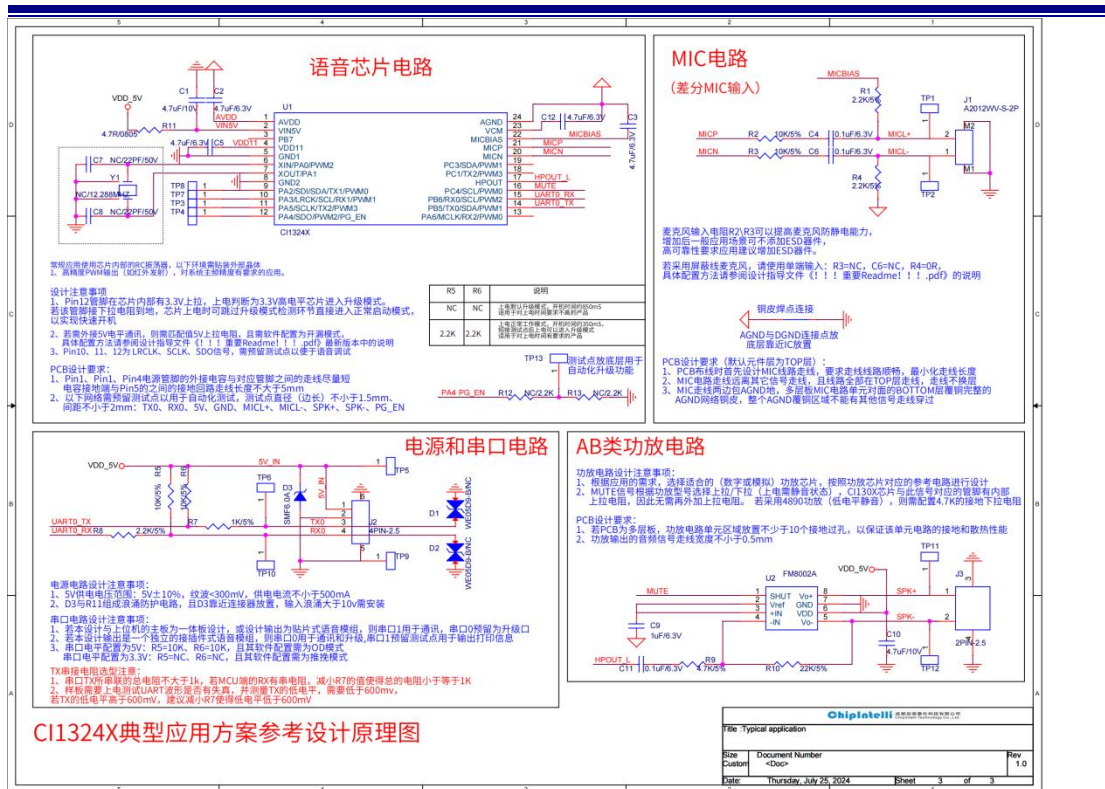


Figure 11: Reference circuit diagram of typical application solution of CI1324X

The figure above shows a typical application circuit diagram of a single microphone differential input and power amplifier output for the CI1324X series chips including CI13241. Users can design according to the corresponding peripheral device specifications in the figure above.

When designing the schematic, consider implementing board-level online upgrade functionality by routing UART0 pins. This allows firmware updates to the chip's internal Flash memory via UART0 after PCB surface-mount components are completed. The PA4 (PG_EN) pin contains a pull-up resistor that defaults to upgrade detection mode during power-on, automatically checking for firmware updates on the UART0 interface. Since the chip's default power-on state is upgrade detection, the startup time after power-on is approximately 850ms. For applications requiring rapid startup, refer to the configuration in Table 5: route PA4 pins and ground them through two 2.2K Ω pull-down resistors. Reserve a test point between these resistors. This design enables immediate normal operation upon power-on, reducing startup time to around 350ms. To enable firmware updates during power-on, externally apply a high-level signal to the test point between the two 2.2K Ω resistors to elevate PA4 pin voltage, allowing firmware updates via UART0.

PG_EN pin external resistor diagram	R5\R6 installation	PG_EN level status	available machine
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	status		time
	R5 and R6 are both NC	high level , Upgrade mode	850ms
	Install 2.2K resistor on R5\R6	low level , work pattern	350ms

Table 5: CI1324X power-on mode configuration table

The CI13241 application design solution can utilize either differential or single-ended microphone inputs, with the differential input configuration recommended in the typical application example. For cost-sensitive implementations, the single-ended input design is preferable to reduce peripheral components. However, this approach is only recommended for microphone input circuits where the total length is less than 20 centimeters. Longer input lines may degrade the microphone's anti-interference capability, ultimately compromising speech recognition performance.

The audio amplifier in the typical application solution adopts AB class amplifier, and it is recommended to use 8002 series amplifier chip. If there is no need for broadcast audio output in the application solution, the amplifier unit circuit can be directly cancelled to reduce the cost of the solution.

If the application solution does not require low power consumption, it is recommended to directly adopt the chip power supply design solution in the typical application solution. If the application solution requires low power consumption design, the 1.1V power supply of the chip can be supplied by external DCDC chip to reduce the operating power consumption of the chip.

The UART communication ports of CI13241 support 5V level communication. In the typical application solution, UART0 communication is designed for 3.3V level communication. If an external 5V communication level is required, simply connect the RX and TX pins of the UART interface to a 5V pull-up resistor.

7.2 Use other precautions

- CI13241 is made of lead-free environmental protection materials. When SMT welding, please set the reflow temperature and time parameters according to lead-free standards.

See Figure 12.

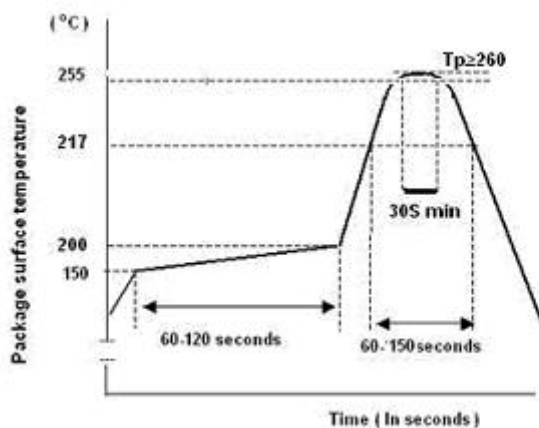


Figure 12: Furnace temperature curve

- Anti-static measures should be taken during the process of taking, handling and processing of CI13241, and its packaging should be made of anti-static materials.

8 History of revision

Table 6: Revision history

RELEASE VERSION	AMENDED CONTENT	DATE OF REVISION
1.0	Initial version	2025.02.27
1.1	1、 Added a section on chip interface description	2025.06.26

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- Chipintelli reserves the right to interpret and modify this specification. If modified, no further notice will be given! Customers should obtain the latest version of the information before application design and verify whether the relevant information is accurate and complete.
 - Any semiconductor product may fail or malfunction under certain conditions. The chip application party is responsible for complying with safety standards and taking safety protection measures when using the product for system design and complete machine manufacturing, so as to avoid personal injury or property loss caused by possible failure of the product!
 - Chipintelli will be committed to providing customers with better products and better services!